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[54] SEMICONDUCTOR DEVICE HAVING POLYSILICON ELECTRODE MINIMIZATION RESULTING IN A SMALL RESISTANCE VALUE

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[58] Field of Search 257/383, 384, 257/412, 413, 344, 903; 437/41, 44, 913

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[57] ABSTRACT

A polysilicon electrode is formed in an active area surrounded by an isolation on a silicon substrate with a gate oxide film sandwiched therebetween, a polysilicon wire is formed on the isolation, and a source/drain region is formed on both sides of the polysilicon electrode. On the both sides of a polysilicon film constituting the electrode and the wire are formed side walls having a height that is ⅘ or less of the height of the polysilicon film. Furthermore, the polysilicon film is provided with a silicide layer in contact with the top surface and portions of the side surfaces of the polysilicon film projecting from the side walls, and another silicide layer is formed in contact with the source/drain region. Since the sectional area of the silicide layer is increased, the resistance value can be suppressed even when the dimension of the polysilicon film is minimized. Thus, the invention provides a semiconductor device including an FET having a low resistance value applicable to a refined pattern.

16 Claims, 23 Drawing Sheets